BIRCH, STEWART, KOLASCH & BIRCH, LLP
INTELLECTUAL PROPERTY LAW
8110 GATEHOUSE ROAD
SUITE 100 EAST
FALLS CHURCH, VA 22042-1248
USA

(703) 205-8000
FAX: (703) 205-8050
(703) 698-8590 (G IV)

e-mail: mailroom@bskb.com
web: http://www.bskb.com

OTHER OFFICES:
CARLSBAD, CALIFORNIA
COSTA MESA, CALIFORNIA
LOS ANGELES, CALIFORNIA

Date: March 25, 2004

Docket No.: 3672-0178PUS1

MS PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As authorized by the inventor(s), transmitted herewith for filing is a patent application applied for on behalf of the inventor(s) according to the provisions of 37 C.F.R. § 1.41(c).

Inventor(s): Robert SCHWEICKERT; and Geirr I. LEISTAD

For: SENSE AMPLIFIER SYSTEMS AND A MATRIX-ADDRESSABLE MEMORY DEVICE PROVIDED THEREWITH

Enclosed are:

☒ A specification consisting of thirty (30) pages

☒ Seven (7) sheet(s) of formal drawings

☐ Applicant claims small entity status under 37 C.F.R. § 1.27

☐ Applicant does not claim priority

☒ Applicant claims the right of priority under the provisions of 35 U.S.C. § 119 and 37 C.F.R. § 1.55(a) based on Application No(s). 2003 1364 filed in Norway on March 26, 2003.
- ☐ Certified copy(ies) is(are) attached hereto.
- ☒ Certified copy(ies) will follow.

☒ Please send correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP or Customer No. 02292
P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____ #39,491
for Michael K. Mutter, #29,680

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

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Attachment(s)

(Rev. 02/13/2004)

sense amplifier system comprising at least one system subblock (SB), and that said at least one system subblock (SB) comprises at least one pseudo-differential sense amplifier circuit (SA) for sensing a polarization state of at least one memory cell (801) during said read operation and at least one pseudo-differential reference sense amplifier circuit (RSA) for sensing a polarization state of at least one reference memory cell (800) during said read operation, said at least one former circuit (SA) being connected with said at least latter circuit (RSA) via a common node (CHREF).

15. A memory device according to claim 14, characterized in that said at least one system subblock (SB) comprises a plurality of said pseudo-differential sense amplifier circuits (SA) for sensing respective polarization states of a corresponding plurality of memory cells (801) during said read operation.

16. A memory device according to claim 14 or claim 15, characterized in that said at least one system subblock (SB) comprises two reference sense amplifier circuits (RSA_1, RSA_2) for sensing two reference memory cells (800) during said read operation, said reference ferroelectric memory cells (800) having opposite polarization states.

17. A memory device according to claim 16, characterized in that the first and the second reference sense amplifier circuits (RSA_1, RSA_2) are adapted for generating an average of a first and a second reference memory cell output signal to said common node (CHREF), and that said at least one sense amplifier circuit (SA) connected therewith is adapted for comparing the output signal at said common node (CHREF) with the output signal from a memory cell (801).

18. A memory device according to claim 14, characterized in that said at least one sense amplifier circuit (SA) and said at least one reference sense amplifier circuit (RSA) are realized with identical amplifier circuitry.

19. A memory device according to claim 18, characterized in that said identical amplifier circuitry (SA, RSA) comprises a reference side and an array side, said reference side mirroring the circuit structure of said array side.